Examining Rambus® Technology

The recent advent of Rambus technology has significantly improved processor access to memory in computer-based designs. This technology is based on a very high-speed, chip-to-chip interface and has been incorporated into new DRAM architectures called **Rambus DRAM or RDRAM®**. It can also be used with conventional processors and controllers to achieve a performance rate that is over 10 times faster than conventional **DRAMs**. Although Rambus systems eliminate the memory access bottleneck, they operate at the fringes of digital performance capability. The Rambus **Channel** transfers data on each edge of a 400-MHz differential clock to achieve an 800-MB/s data rate. Moreover, the data, clock and control lines have 800-mV logic levels that must operate in a strictly controlled impedance environment and meet **specific high-speed** timing requirements.

Design Requirements

While offering many advantages, the Rambus **memory** architecture creates three major system design and verification challenges for the system developer. First, there are strict requirements imposed by the Rambus **Channel's** high-speed signals. The 26 high-speed, high-quality signals must travel on controlled-impedance transmission lines that are closely matched in length to minimize timing skew. These signals form the active part of the Rambus **Channel** when transferring information and interact with standard CMOS circuits using a special 800-mV logic level. This streamlined structure makes it complicated to examine real-time system interactions with a scope or logic analyzer. To get a good look at what is going on the Rambus **Channel**, the designer has to sift through a welter of high-speed information carried on all 13 lines to verify performance and characterize the operation of the system.

The logical signals used in the Rambus **Channel** pose some **new requirements** for the system designer due to their small logic swing and fast transitions. All devices in the system receive these low-voltage swing signals through a differential input circuit. The rise-time characteristic for clock and data signals is recommended to be no slower than 250 ps. Furthermore, since there are no "output enable" signals piped around and each line is a wired OR structure, any line can be pulled down to a "1" by any element on the bus.

The second challenge has to do with the timing requirements resulting from the synchronous nature of the data transfer on the Rambus **Channel** and its high-speed operation. Because clock and data skew must be carefully matched

to ensure proper operation, the 400-MHz clock and data must travel along nearly identical paths both to and from the Master. Data is transferred on both rising and falling edges of the 400-MHz clock, resulting in a **1.6GB/s** data transfer rate. Each data transfer occurs on a 1.25-ns interval determined by a rising or falling edge. With information moving at this rate, there is little margin for error.

The third challenge is created by the logical layer of the Rambus **Channel**, which consists of the data transfer between the master (e.g., a CPU) and slave. Data is transferred throughout a Rambus system in blocks. These blocks are moved in transactions made up of three types of packets — request, acknowledge and data packets.

High-Speed Verification Required

To verify overall system timing for the Rambus **memory** architecture in a design, the engineer will need to rely on the TDS 694C to verify the extremely high-speed signal characteristics single shot. Its full 3-GHz bandwidth on each channel and 120k points per channel ensures all the details will be captured and displayed. The TLA 700 series logic analyzers will also be invaluable for observing the intricate and detailed interaction between the Rambus control signals and the data flow. These logic analyzers not only provide hundreds of channels for observing all of the Rambus outputs simultaneously, but also have the bandwidth and resolution to create an accurate picture of the bus' operation.

When viewing these high-speed signals, probe loading and skew management are the two biggest issues, making high-impedance, low-capacitance probes a must. New active probes just introduced by Tektronix complement the TDS 694C capabilities by supporting a system bandwidth at the probe tip of up to 3 GHz. With remarkably low loading — only 1 pF with 20 kΩ loading — designers can rest assured that what they are seeing displayed on the oscilloscope truly represents the Rambus signal activity. In addition, a new 1.7-GHz* active differential probe, the P6248, was designed specifically for digital designs that utilize a high-speed differential clock (1X providing 1.7GHz and 10X providing 1.85 GHz [1X and 10X – typical probe only]). And the high-density, controlled-impedance probing solution for the TLA 700 ensures the faithful acquisition and display of high-speed signals.

One of the most important components in characterizing and testing Rambus system design is system stimulation. The designer needs to simulate system operation by creating typical master signals to verify device operation under worst-case timing conditions. This requires a signal generator that can generate flexible output with extremely precise timing. With this generator,

the designer can precisely program the skew of the Rambus NRZ signals to verify that the RDRAM components work across all legal input timings.

Only the Tektronix DG2040, with its unique 1.1-GHz data generation capabilities and ±100-ps resolution, provides the kind of generated output needed to simulate the master RDRAM bus device for worst-case clock conditions and worst-case clock/data timing conditions. The output stage of a DG2040 acts very much like an RDRAM device. Its output channel can be programmed to pull down to Vhigh through a source impedance of 50 ohms and the NRZ signal type used to simulate the synchronous nature of an RDRAM device. Since the Rambus **Channel** uses a wired OR topology, no "TRISTATE" is required to have the master release and the slave take over the bus.

The DG2040 can be used in conjunction with the TDS 694C's jitter analysis software, creating a fully functional jitter generator/analysis system. A deep memory of 256 K bits behind both of the generator's outputs allows long complex data patterns to be created. The edge control in the generator enables the designer to retard or advance by ±100 ps in 5-ps steps or continuously jitter the relative timing of the selected edges of the data stream. This feature is particularly useful when evaluating setup and hold-time margins, injecting clock jitter into a digital circuit or evaluating conditions of meta-stability. This edge control function also permits an external modulating signal to continuously jitter selected edges by up to ±100 ps — a valuable capability for evaluating the effects of jitter on the Rambus system.

A Productive Strategy

Incorporating the Rambus **memory** architecture into an advanced digital design gives next-**generation** processors the high-speed access to memory they require. To verify whether this extremely sophisticated bus technology is performing as it should, designers can rely on Tektronix' integrated set of test and measurement tools. By using the leading-edge TDS 694C oscilloscope in tandem with the TLA 700 series logic analyzers and the DG2040 generator, designers can quickly and effectively address any system design and characterization challenges related to using the Rambus technology.

*The P6248 is **guaranteed** at 1.5 GHz over the operating temperature range – O C to 50 C. The probe typically will have a 1.70 GHz (1X) and 1.85 (10X) bandwidth at room temperature, 23 C to 27 C.